12.4 Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies

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Two side effects of technology scaling that have a significant impact on analog circuit design are the reduced signal swing and the decrease in intrinsic device gain. Gain is important in feedback-based analog signal-processing systems, because it determines the accuracy of the output value. Cascoded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swings of scaled technologies. An alternative method for achieving high gain in an operational amplifier without reducing signal swing is to cascade several lower-gain amplifiers. Nested-Miller compensation approaches [1] can be used to stabilize the cascaded feedback system, but the frequency response of the closed-loop system is significantly sacrificed to ensure stability. A recent development in the area of pipeline ADCs avoids these problems by using open-loop amplifiers with digital calibration to compensate for the gain variation [2]. In this paper, a comparator-based switched-capacitor (CBSC) circuit design methodology is described that eliminates the use of opamps in sampled-data systems.

A sampled-data system typically operates in two phases, a sampling phase (ϕ_1) and a charge-transfer phase (ϕ_2). An important property of these systems is that the output voltage needs to be accurate only at the moment the output is sampled. No constraint is placed on how the stage gets to the final output value. Feedback systems use a high-gain opamp to force a virtual-ground condition at the opamp input. The top circuit in Fig. 12.4.1 shows the conventional opamp-based switched-capacitor gain stage. The bottom circuit in Fig. 12.4.1 shows the proposed CBSC approach in conceptual form, where a comparator and a current source have replaced the opamp. Assuming the comparator input V_x starts below the common-mode voltage at V_{xo}, the current source charges the output circuit until the comparator detects the virtual-ground condition and turns the current source off. At this instant, the output is sampled on C_L. Because the CBSC design ensures the same virtual-ground condition as the opamp-based design, both circuits produce the same output value at the sampling instant.

A more practical CBSC gain stage can be designed using a dual-ramp charge-transfer phase and a comparator-controlled sampling switch. A schematic diagram of this circuit is shown in Fig. 12.4.2. Assume that the input (V_{in}) has been sampled onto the parallel combination of C_1 and C_2 in the previous sampling phase. At the beginning of the charge-transfer phase, a brief preset (P) of the stage must be performed to clear C_L and ensure V_x starts below the common-mode voltage. The preset can be accomplished by momentarily pulling the output node to the lowest potential in the system (V_{ss}). Next, the coarse charge-transfer phase (E_1) begins. Current source I_1 results in a relatively fast voltage ramp on V_x toward V_{CM}. At this point, the comparator makes its first decision. Because the comparator has a finite delay, I_1 turns off after V_x crosses V_{CM}. After I_1 turns off, current source I_2 turns on to begin the fine charge-transfer phase (E_2). The current I_2 is less than I_1 and results in a slower ramp back toward V_{CM}. When the ramp at V_x crosses V_{CM} again, the sampling switch (S) is opened after the brief delay of the comparator. The correct charge is sampled on C_L at that moment. Therefore, the signal S defines the sampling instant. The final overshoot from the comparator delay is a constant offset in the output if the ramp rate and comparator delay are constant. The current source I_2 turns off a short time after the switch opens, but this does not affect the sampled value. Preliminary analysis indicate CBSC circuits are more power efficient than conventional opamp-based circuits, because detecting the virtual-ground condition is more energy efficient than forcing the virtual ground.

The CBSC concept is general and can be applied to any sampled-data analog circuit. For example, the CBSC design approach can be applied to a pipelined ADC signal path, as shown in Fig. 12.4.3. The comparator now controls both the sampling switch and the strobe time for the bit-decision comparators. A prototype CBSC pipeline ADC is constructed and operates similar to the opamp version of the ADC. Figure 12.4.4 shows a simplified schematic of the first two stages of the prototype CBSC 1.5b/stage pipeline ADC.

To make its decisions quickly, the comparator must have a large gain and minimum delay. Unlike the opamp, the comparator can achieve the required gain with the cascade of several low- to moderate-gain stages without concern for stability in feedback. Figure 12.4.5 shows the schematic of the comparator used in the pipeline. The first stage is a band-limited stage to minimize the noise in the comparator decision. Two diode-connected NMOS devices clamp the output swing for faster recovery. Following the band-limiting stage is a cascade of three broadband low-gain differential amplifier stages with PMOS triode loads. The first two stages have their output dc levels shifted down by a diode connected PMOS transistor. The third stage can then generate the larger swing required to drive the level-converting stage. The level converter is used to generate the rail-to-rail signals required to drive the logic for the sampling switches and current sources.

A prototype CBSC pipeline ADC is implemented in a 0.18μm CMOS technology. The active die area of the ADC is 1.2mm^2. The INL and DNL plots for the 10b converter are shown in Fig. 12.4.6. At an 8MHz sampling frequency, the DNL is +0.33/-0.28LSB, and the INL is +1.59/-1.13LSB. The input-referred rms noise is 0.65LSB. The core ADC power consumption of all 10 stages of the pipeline converter is 2.5mW from a 1.8V supply, resulting in a 0.3pJ/b FOM. For this first proof-of-concept chip, no attempt is made for power optimization. For example, 10 identical stages are cascaded without scaling. Further improvement of the FOM should be possible by techniques such as comparator power optimization and stage scaling. The micrograph of the test chip is shown in Fig. 12.4.7.

Acknowledgements:
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References:
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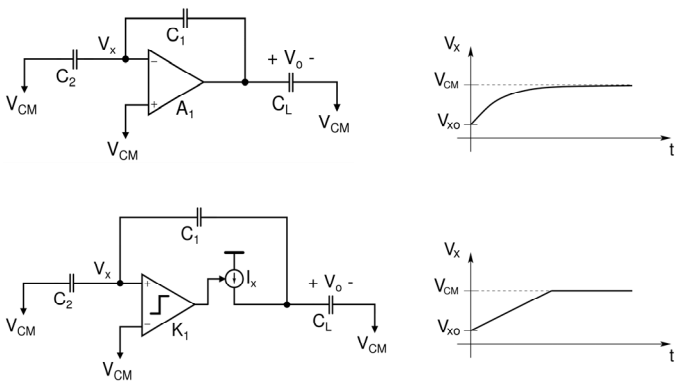

Figure 12.4.1: Opamp versus comparator-based switched-capacitor (CBSC) gain stage.

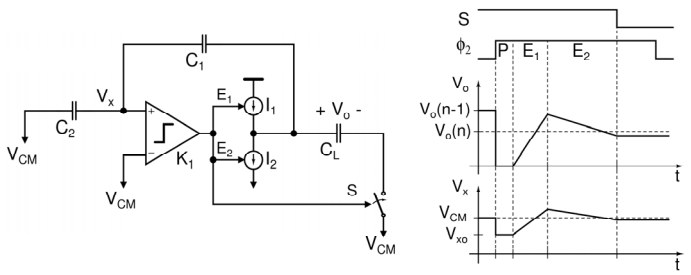

Figure 12.4.2: CBSC charge transfer phase (ϕ_2) using dual-ramp settling. Sampling phase (ϕ_1) not shown.

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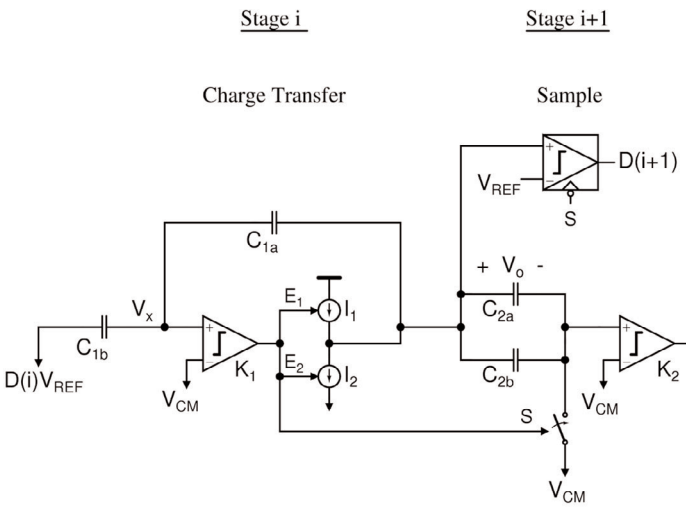

Figure 12.4.3: CBSC pipeline stage.

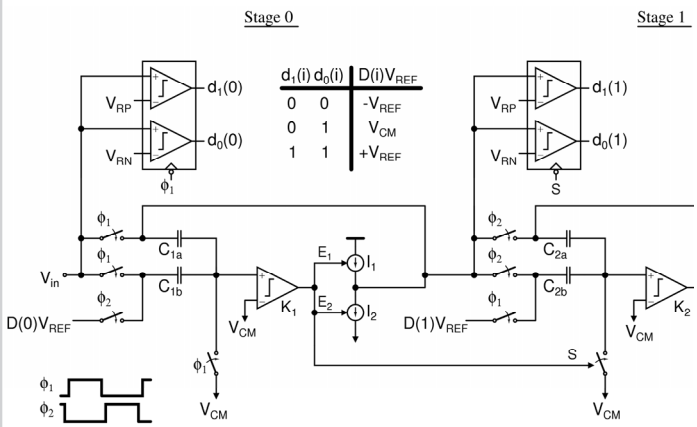

Figure 12.4.4: First two stages of CBSC 1.5b/stage pipeline ADC.

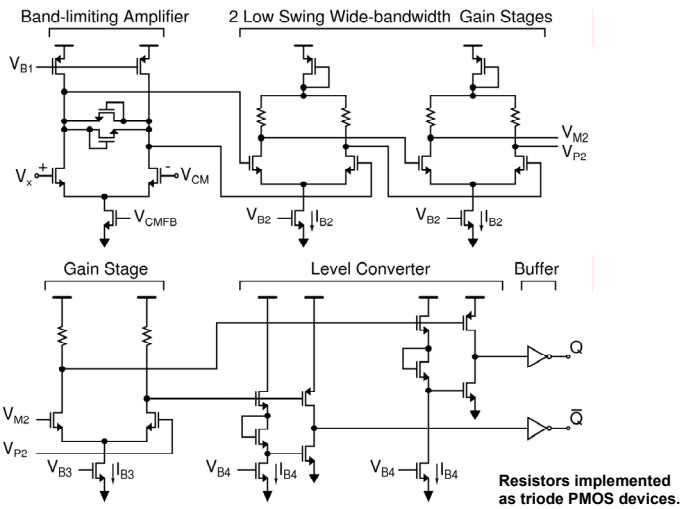

Figure 12.4.5: Continuous-time comparator schematic.

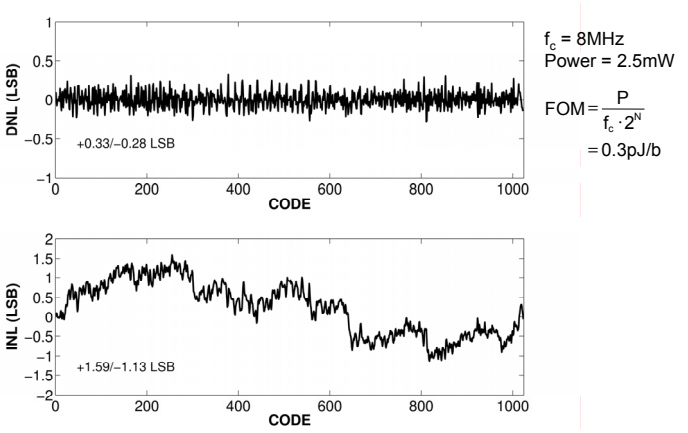

Figure 12.4.6: Measured INL and DNL of 8MHz 10b CBSC pipeline ADC.

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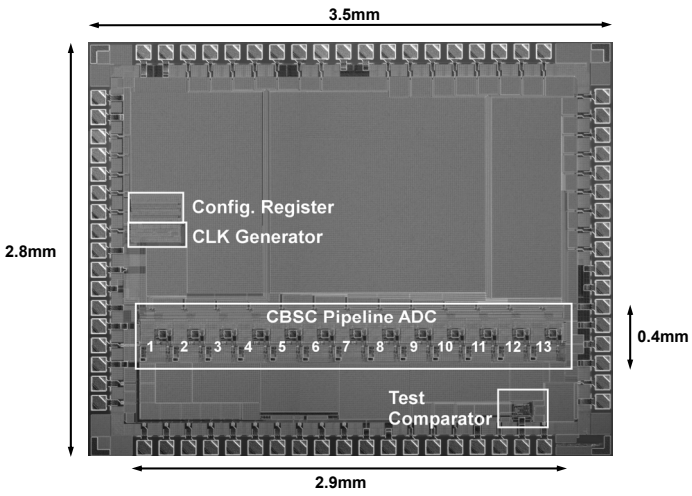

Figure 12.4.7: CBSC ADC chip micrograph. ADC active die area is 1.2mm^2.

